CONCOURS EXTERNE D'ACCES AU CORPS DES TECHNICIENS DE RECHERCHE ET DE FORMATION DU MINISTERE DE L'ENSEIGNEMENT SUPERIEUR, DE LA RECHERCHE ET DE L'INNOVATION

B.A.P. C

Emploi-type : Technicien-ne électronicien-ne

Epreuve écrite d'admissibilité

Date : 25.05.2021
Durée : 3 heures
Coefficient : 3

L'épreuve comporte 41 pages dont 23 pages de sujet et 18 pages d'annexes.

Veuillez vérifier en début d'épreuve s'il est complet et signaler toute anomalie.

Toutes les réponses aux questions doivent être portées directement sur le sujet. Vous répondrez aux questions en respectant les emplacements réservés à cet effet et en soignant la présentation. Vous devez écrire à l'encre bleue ou noire (sont interdits l'encre de couleur rouge, verte et le crayon à papier).

Les calculatrices sont autorisées (programmable ou non). Aucun document n'est autorisé : sont interdits les téléphones portables, baladeurs audio, tablettes, montres connectées et tout autre document à l'exception du sujet.

/! Il est interdit aux candidats de signer leur composition ou d'y mettre un signe quelconque pouvant indiquer sa provenance.

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Emploi type : technicien-ne électronicien-ne
- Session 2021 –

Nom : ……
Nom de Jeune Fille : ……
Prénom : ……
Né(e) le : ……..

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Emploi type : technicien-ne électronicien-ne
- Session 2021 –

Note : / 20

Partie 1 : Électronique Analogique

Question 1.1 : Impédance et relation entre tension et courant

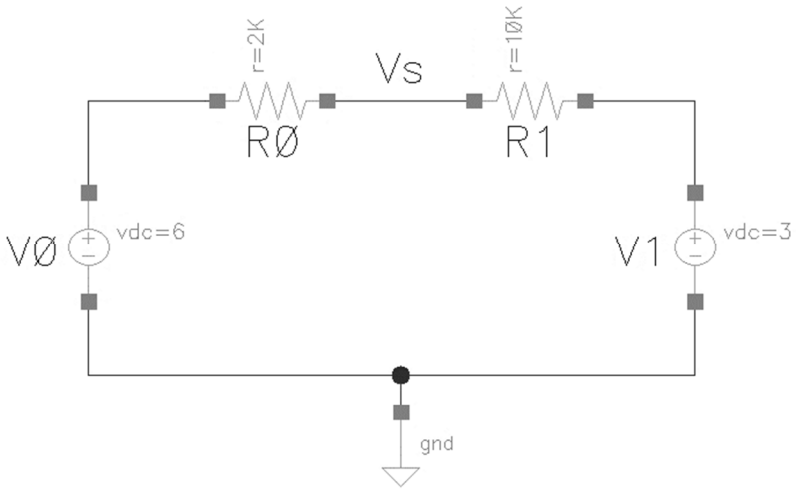
Donner l'impédance et la relation courant tension des composants ci-dessous :

Résistance	**Bobine**
U= Z=	U= Z=
Condensateur	**Diode**
I= Z=	I=

NE RIEN ECRIRE DANS LA PARTIE BARRÉE

Question 1.2 : Calcul dans les circuits

À l'aide du théorème de superposition, donner l'expression de la tension Vs en fonction de tous les éléments du montage ci-dessous. Faire l'application numérique avec V_0=6V, V_1=3V, R_0=2kΩ, R_1=10kΩ.



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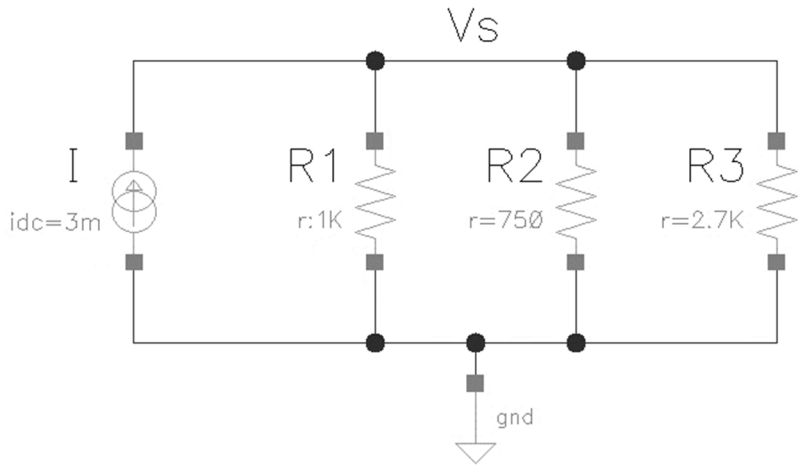
À l'aide du diviseur de courant, donner les expressions des courants I_{R1}, I_{R2} et I_{R3}. Donner également l'expression de Vs.

Faire l'application numérique avec I=3mA, R_1=1kΩ, R_2=750Ω, R_3=2.7kΩ.



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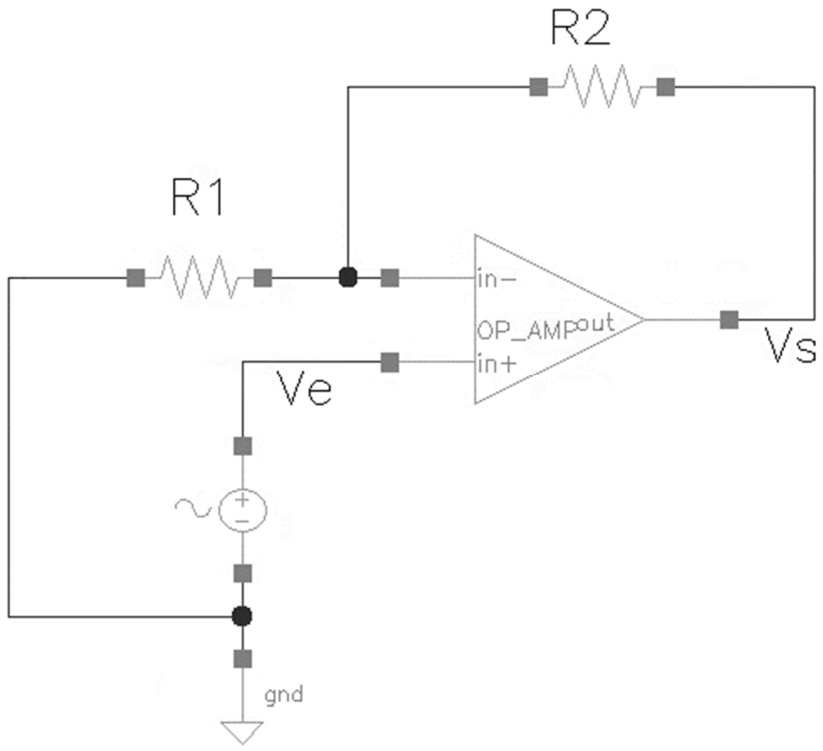
Question 1.3 : Amplification

On souhaite amplifier sans inverser un signal Ve d'un facteur 100. L'amplificateur utilisé est un TL081C (voir documentation technique en annexe). Le montage utilisé est représenté ci-dessous :



Le signal Ve s'écrit sous la forme $Ve = 0.05 \times sin(2\pi \times 1500 \times t + \varphi)$. Quel est la valeur crête à crête du signal Ve et quelle est sa fréquence ?

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Comment s'appelle ce montage ?

_____

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En vous aidant de la documentation technique, répondez aux questions ci-dessous :

Tension d'offset maximale	
Slew Rate typique	
Produit Gain Bande passante typique	

Donner l'expression de la fonction de transfert Vs/Ve en fonction de R_1 et R_2 en considérant que l'AOP est idéal.

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Choisir les résistances R_1 et R_2 pour obtenir un gain de 100.

_____

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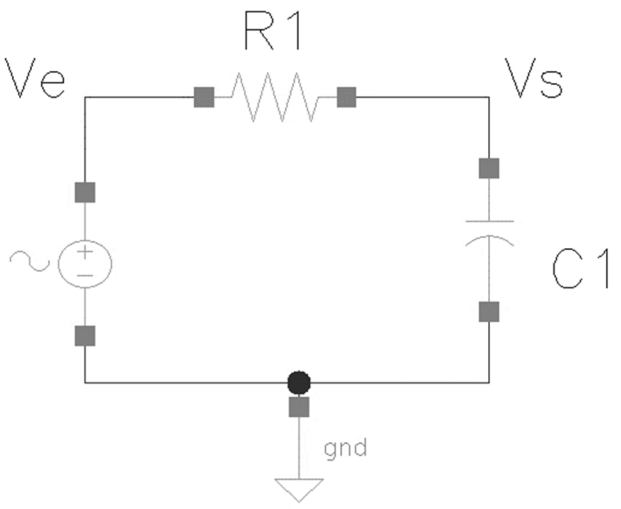
NE RIEN ECRIRE DANS LA PARTIE BARRÉE

Question 1.4 : Filtrage passif

On souhaite filtrer un signal sinusoïdal. Pour cela, on utilise le filtre ci-dessous :



Quelle est la nature de ce filtre (passe-bas, passe-haut, …) ?

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Quelle est l'ordre de ce filtre ?

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NE RIEN ECRIRE DANS LA PARTIE BARRÉE

Donner l'expression de la fonction de transfert H(jw)=Vs(jw)/Ve(jw) et la mettre sous la forme :

$$H(jw) = \frac{Ao}{1 + j\frac{w}{wo}}$$

Par identification, donner l'expression du gain Ao et de la fréquence de coupure fo de ce filtre :

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Donner l'expression du module de la fonction de transfert |H(jw)|. On rappelle que :

$$Pour\ z = a + jb \rightarrow |z| = \sqrt{a^2 + b^2}$$

$$\left|\frac{z_1}{z_2}\right| = \frac{|z_1|}{|z_2|}$$

Donner l'expression de l'argument de la fonction de transfert |H(jw)|. On rappelle que :

$$\arg(a + jb) = \arctan(\frac{b}{a})$$

$$arg(\frac{z_1}{z_2}) = \arg(z_1) - \arg(z_2)$$

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Tracer le diagramme de Bode asymptotique (gain et phase) sachant que :

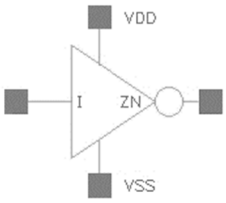
$$Av_{dB}(w) = 20 \times \log|H(jw)|$$
$$\phi(w) = \arg(H(jw))$$

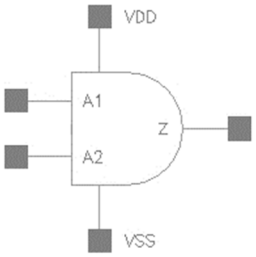
NE RIEN ECRIRE DANS LA PARTIE BARRÉE

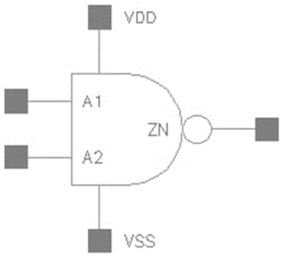
Partie 2 : Électronique Numérique

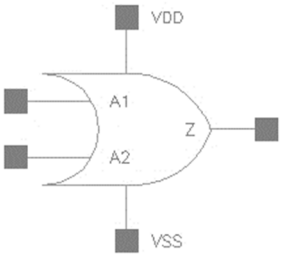
Question 2.1 : Porte logique

Donner la table de vérité des portes logiques ci-dessous :









NE RIEN ECRIRE DANS LA PARTIE BARRÉE

On souhaite mesurer le temps de propagation de la porte inverseuse. Pour cela, on utilise le composant 74LS04 (voir annexes).

Combien y a t-il de portes logiques dans un boîtier ?

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_____

D'après la documentation technique, quels sont les temps de propagation de cet inverseur ? Dans quelles conditions sont-ils obtenus ?

_____

_____

_____

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On souhaite vérifier la valeur donnée par la documentation technique en effectuant une mesure. Pour cela, on utilisera toutes les portes logiques du boîtier. La sonde de mesure dont nous disposons a les caractéristiques suivantes :

Sonde ×1	Rsonde=1MΩ	Csonde=72pF
Sonde ×10	Rsonde=10MΩ	Csonde=18pF

Vaut-il mieux utiliser une sonde × 1 ou une sonde × 10. Justifier votre réponse.

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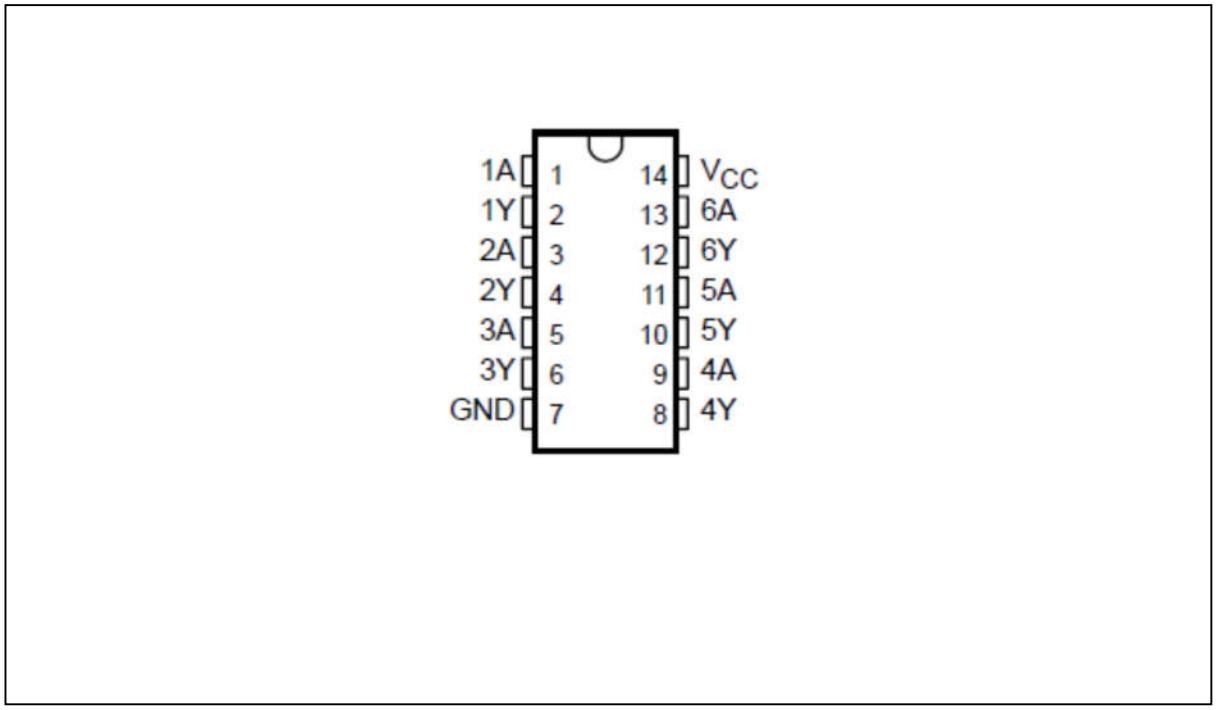
NE RIEN ECRIRE DANS LA PARTIE BARRÉE

Proposez un schéma de câblage en se plaçant à Vcc nominale. On ne prendra en compte que l'impact de la sonde.



Après mesures, on obtient un temps de propagation tplh à la sortie du dernier inverseur de 54ns. Le comparer à la documentation technique et conclure.

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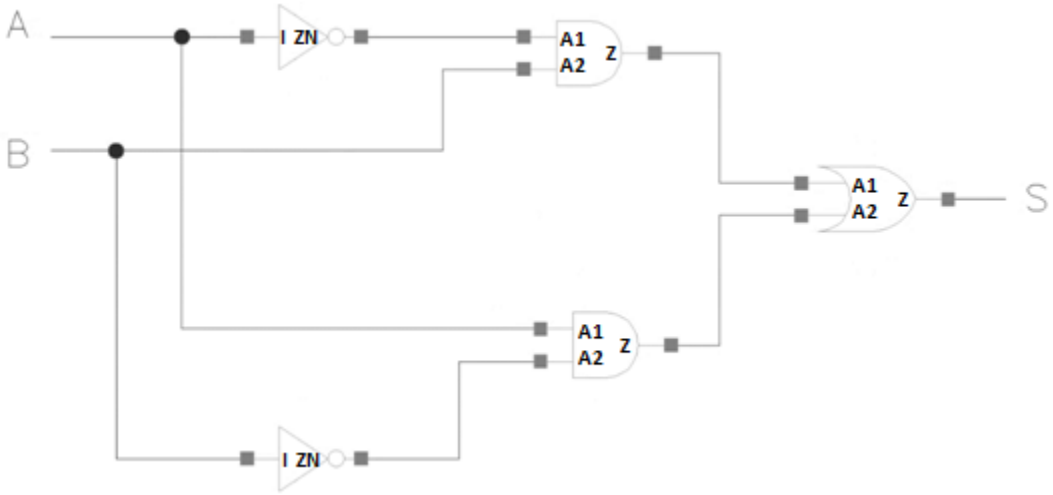
NE RIEN ECRIRE DANS LA PARTIE BARRÉE

Exercice 2.2 : Logique combinatoire

Donner l'équation de la sortie S en fonction des entrées A et B du montage ci-dessous :



Donner la table de vérité correspondant à cette équation :

NE RIEN ECRIRE DANS LA PARTIE BARRÉE

En déduire un schéma simplifié du montage :

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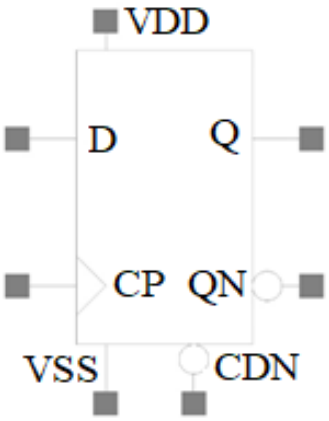
Exercice 2.3 : Logique séquentielle

Quelle est le nom de la bascule ci-dessous ?



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Sur quel front de l'horloge la bascule fonctionne elle ? Justifiez :

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Donner la table de vérité de cette bascule :

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On réalise le montage suivant. Le signal d'entrée est un signal carré allant de 0 à 1.2V et de fréquence 1kHz.

Quelle valeur de tension faut-il mettre sur CDN (Reset) pour que le circuit fonctionne normalement ?

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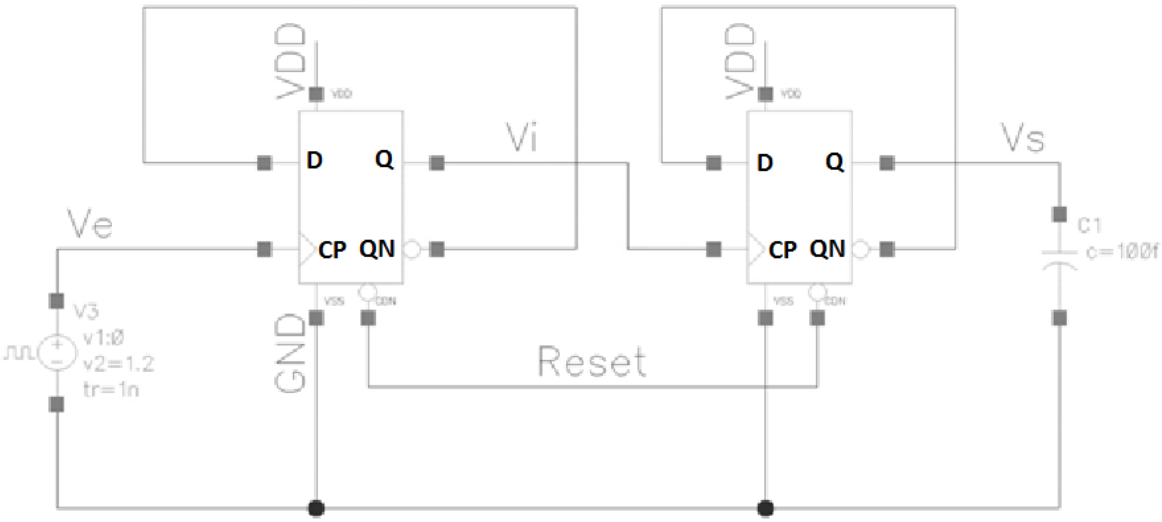

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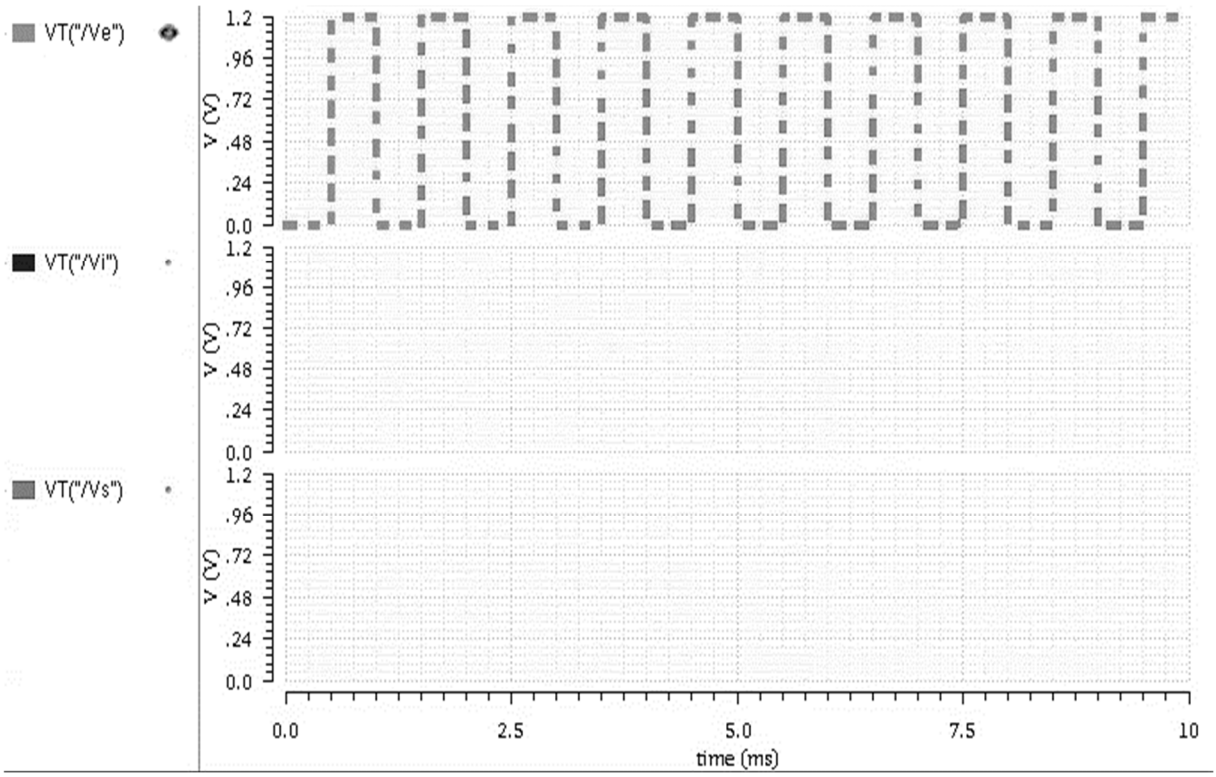
Tracer le chronogramme et expliquer la fonction de ce montage :



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Partie 3 : CAO et mesures

Exercice 3.1 : Généralités

Que signifie l'acronyme CAO ?

_____

_____

_____

Que signifie l'acronyme CMS ?

_____

_____

_____

Citez 2 logiciels de conception de circuits imprimés :

_____

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_____

D'après la netlist ci-dessous, retrouver le schéma équivalent avec la valeur des composants :

```
R1 Vs Ve 1k
R2 0 Vs 2k
V1 Ve 0 2
.backanno
.end
```

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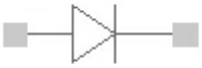
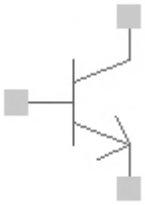
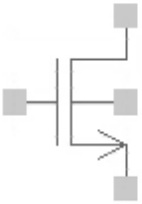
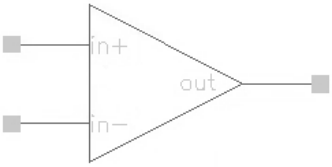
NE RIEN ECRIRE DANS LA PARTIE BARRÉE

Exercice 3.2 : Lectures de schémas

Donner le nom des composants ci-dessous :

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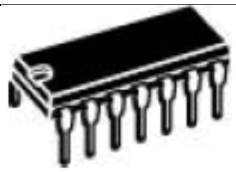
Exercice 3.3 : Types de boîtiers

Remplissez le tableau ci-dessous concernant les noms de boitier :

Type de boitier	Nom
	
	
	
	

Exercice 3.4 : Lecture de valeurs de résistances

Donner les valeurs des résistances ci-dessous :

Code couleur	Marron-noir-rouge-or	Jaune-violet-marron-or	Gris-rouge-orange-or
Valeurs nominales			
Valeurs minimales			
Valeurs maximales			

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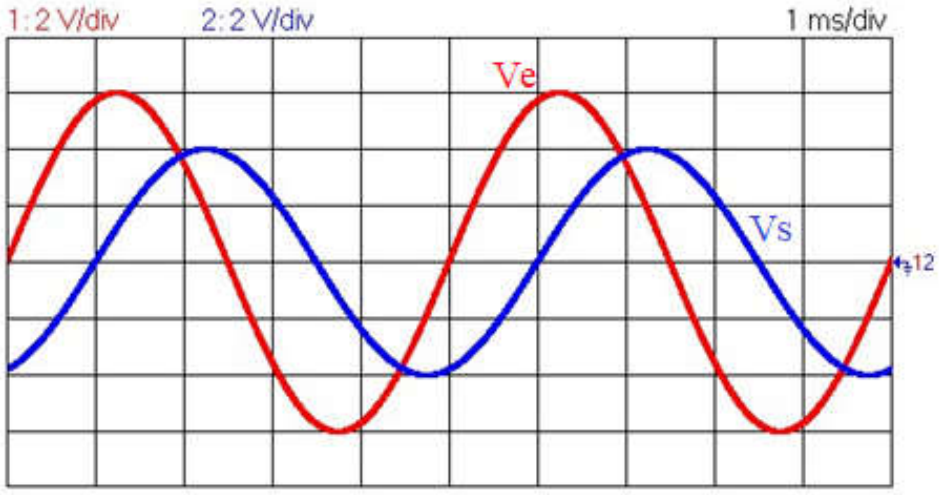
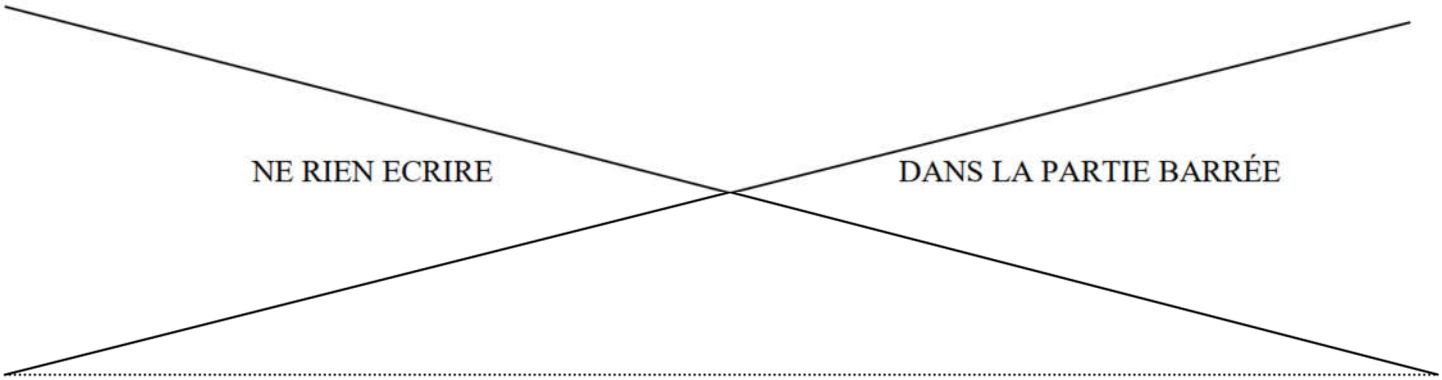
Exercice 3.5 : Lecture de signaux à l'oscilloscope

On observe les signaux suivant sur un oscilloscope. Remplir le tableau ci-dessous :



	Ve	Vs
Amplitude		
Fréquence		
Déphasage $\lvert\varphi_{Vs/Ve}\rvert$		
Tension efficace		
Tension moyenne		



Partie 4 : Anglais

Exercice 4.1 : Traduire le texte ci-dessous en français

Hi Denis,
Our company would like to order you again two radio communication boxes for drones. Your service had already done this last year so there won't be any new development to do, it's just a production task.

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Exercice 4.2 : Traduire le texte ci-dessous en anglais

Nos délais sont assez serrés, aussi voudrions-nous le produit définitif pour dans deux mois. Quand pourrions-nous nous rencontrer pour une première réunion?
Par ailleurs, pourriez-vous nous envoyer rapidement un devis pour la réalisation de ces deux circuits électroniques et de leurs boîtiers, en prenant en compte quantitativement les divers éléments nécessaires pour leur réalisation.

Cordialement,

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Annexes

Documentation technique du 74LS04

SN5404, SN54LS04, SN54S04,
SN7404, SN74LS04, SN74S04
HEX INVERTERS

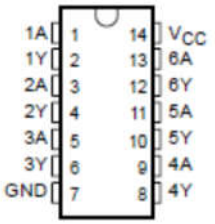
SDLS029B – DECEMBER 1983 – REVISED FEBRUARY 2002

- Dependable Texas Instruments Quality and Reliability

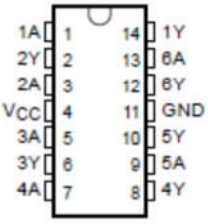
description

These devices contain six independent inverters.

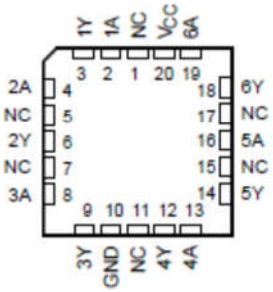
SN5404 . . . J PACKAGE
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404 . . . D, N, OR NS PACKAGE
SN74LS04 . . . D, DB, N, OR NS PACKAGE
SN74S04 . . . D OR N PACKAGE
(TOP VIEW)



SN5404 . . . W PACKAGE
(TOP VIEW)



SN54LS04, SN54S04 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

ORDERING INFORMATION

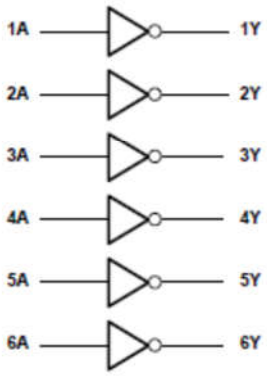
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN7404N	SN7404N
		Tube	SN74LS04N	SN74LS04N
		Tube	SN74S04N	SN74S04N
	SOIC – D	Tube	SN7404D	7404
		Tube	SN74LS04D	LS04
		Tape and reel	SN74LS04DR	
		Tube	SN74S04D	S04
		Tape and reel	SN74S04DR	
	SOP – NS	Tape and reel	SN7404NSR	SN7404
		Tape and reel	SN74LS04NSR	74LS04
	SSOP – DB	Tape and reel	SN74LS04DBR	LS04
–55°C to 125°C	CDIP – J	Tube	SN5404J	SN5404J
		Tube	SNJ5404J	SNJ5404J
		Tube	SN54LS04J	SN54LS04J
		Tube	SN54S04J	SN54S04J
		Tube	SNJ54LS04J	SNJ54LS04J
		Tube	SNJ54S04J	SNJ54S04J
	CFP – W	Tube	SNJ5404W	SNJ5404W
		Tube	SNJ54LS04W	SNJ54LS04W
		Tube	SNJ54S04W	SNJ54S04W
	LCCC – FK	Tube	SNJ54LS04FK	SNJ54LS04FK
		Tube	SNJ54S04FK	SNJ54S04FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each inverter)

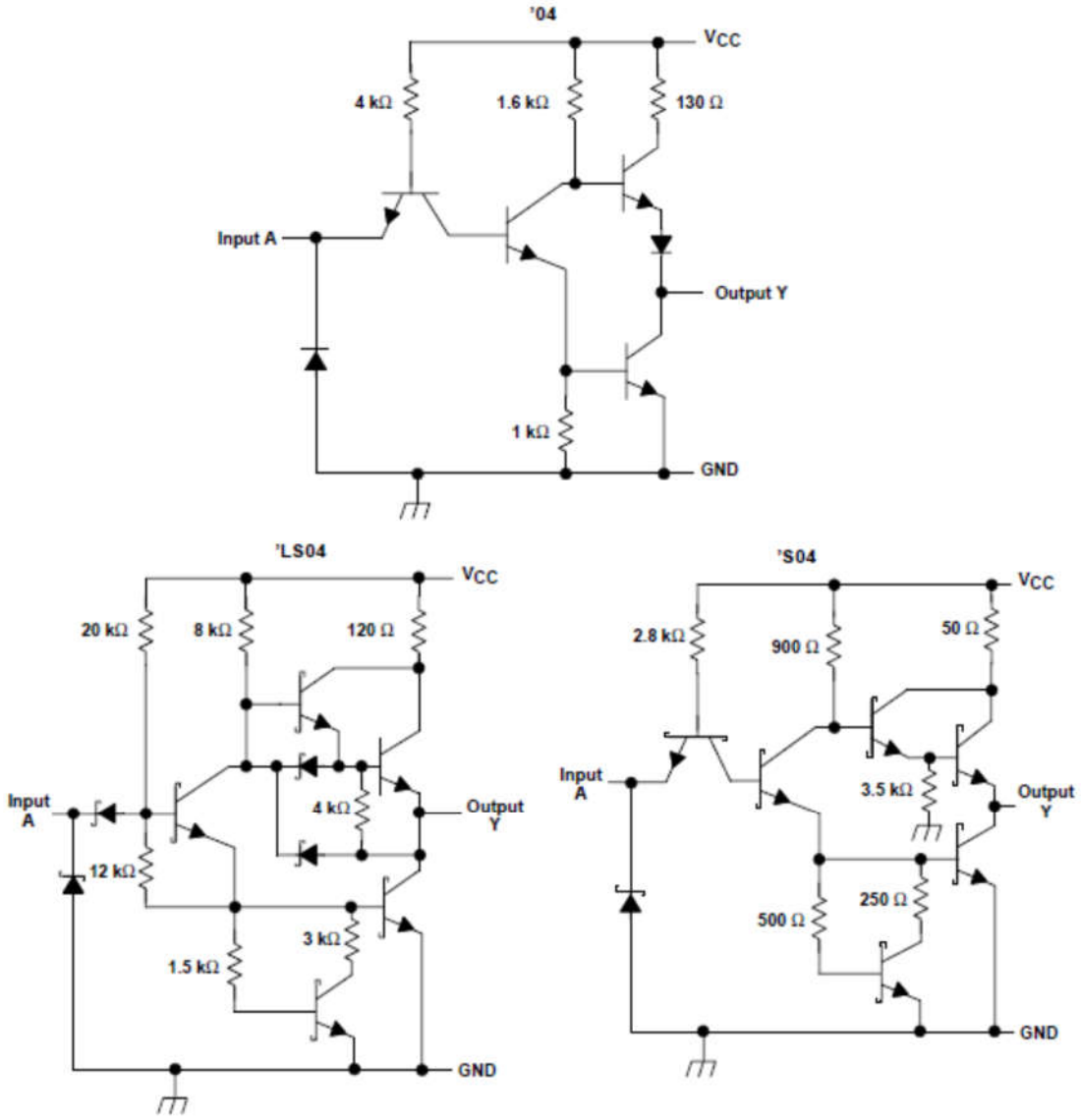
INPUT A	OUTPUT Y
H	L
L	H

logic diagram (positive logic)



$Y = \overline{A}$

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I: '04, 'S04 ..... 5.5 V
'LS04 ..... 7 V
Package thermal impedance, θ_{JA} (see Note 2): D package ..... 86°C/W
DB package ..... 96°C/W
N package ..... 80°C/W
NS package ..... 76°C/W
Storage temperature range, T_{stg} ..... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		SN5404			SN7404			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–0.4			–0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡			SN5404			SN7404			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	V_{CC} = MIN,	I_I = –12 mA				–1.5			–1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OH} = –0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.4 V				40			40	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				–1.6			–1.6	mA
I_{OS}¶	V_{CC} = MAX			–20		–55	–18		–55	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			6	12		6	12	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			18	33		18	33	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		SN5404 SN7404			UNIT
					MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 400 Ω,	C_L = 15 pF		12	22	ns
t_{PHL}						8	15	

recommended operating conditions

		SN54LS04			SN74LS04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–0.4			–0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54LS04			SN74LS04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = –18 mA				–1.5			–1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = MAX,	I_{OH} = –0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V	I_{OL} = 4 mA		0.25	0.4			0.4	V
			I_{OL} = 8 mA					0.25	0.5	
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				20			20	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				–0.4			–0.4	mA
I_{OS}§	V_{CC} = MAX			–20		–100	–20		–100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			1.2	2.4		1.2	2.4	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			3.6	6.6		3.6	6.6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		SN54LS04 SN74LS04			UNIT
					MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 2 kΩ,	C_L = 15 pF		9	15	ns
t_{PHL}						10	15	

recommended operating conditions

		SN54S04			SN74S04			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

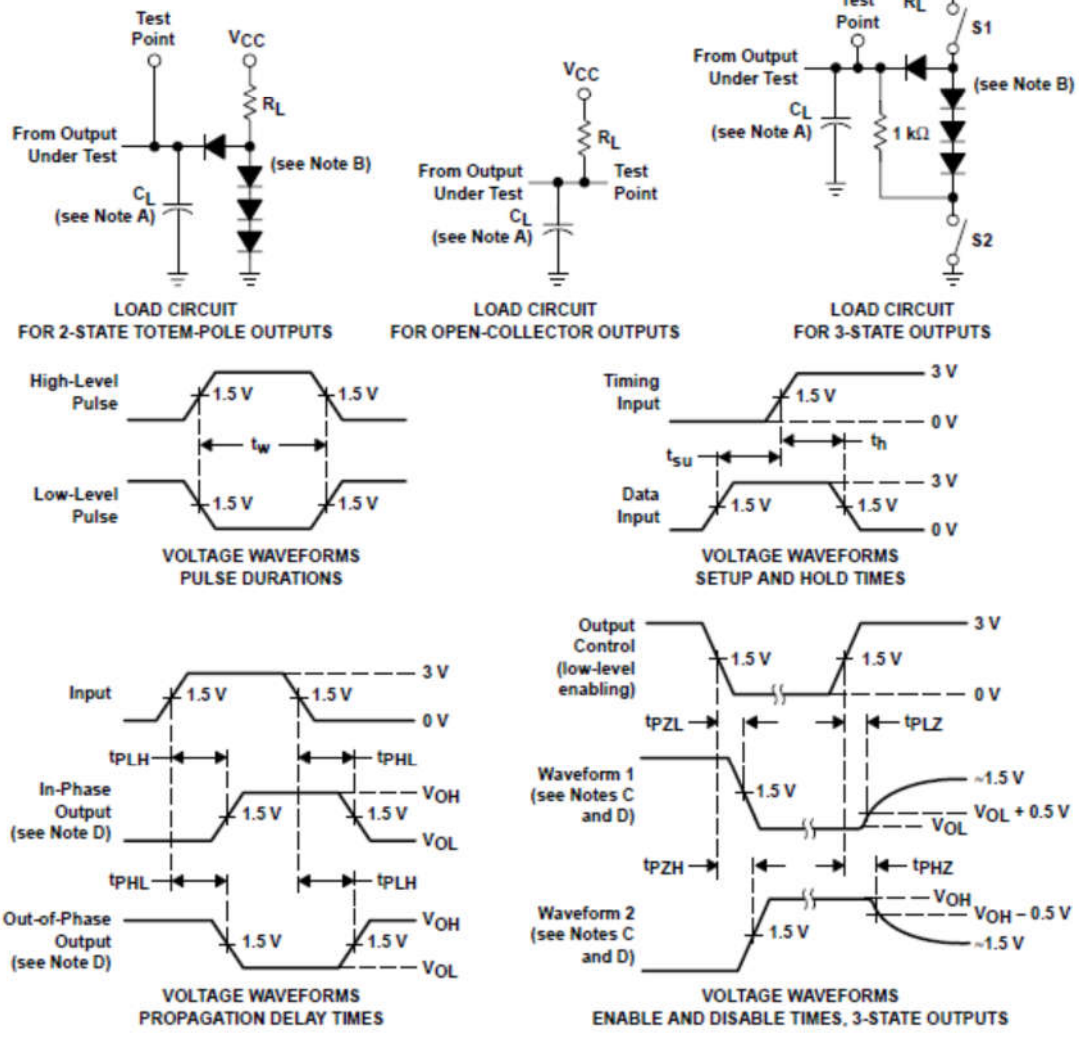
PARAMETER	TEST CONDITIONS†			SN54S04			SN74S04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 20 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				50			50	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V				−2			−2	mA
I_{OS}§	V_{CC} = MAX			−40		−100	−40		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			15	24		15	24	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			30	54		30	54	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		SN54S04 SN74S04			UNIT
					MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 280 Ω,	C_L = 15 pF		3	4.5	ns
t_{PHL}						3	5	
t_{PLH}	A	Y	R_L = 280 Ω,	C_L = 50 pF		4.5		ns
t_{PHL}						5		

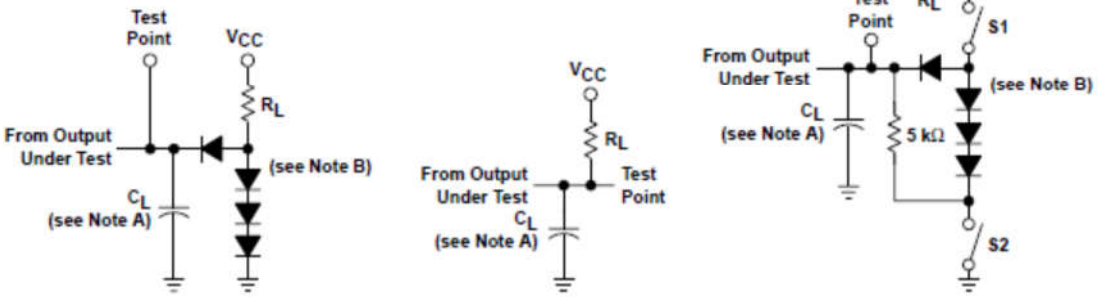
PARAMETER MEASUREMENT INFORMATION
SERIES 54/74 AND 54S/74S DEVICES

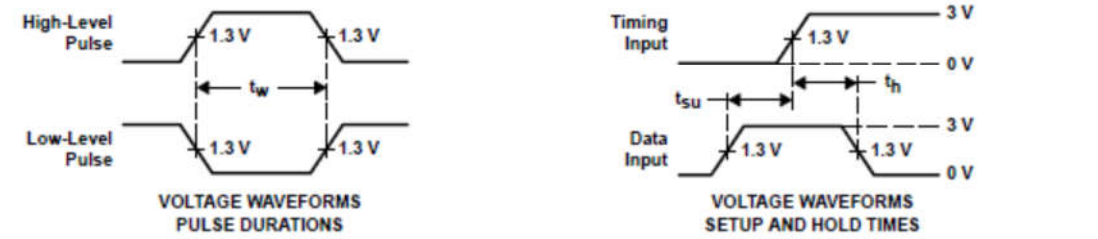


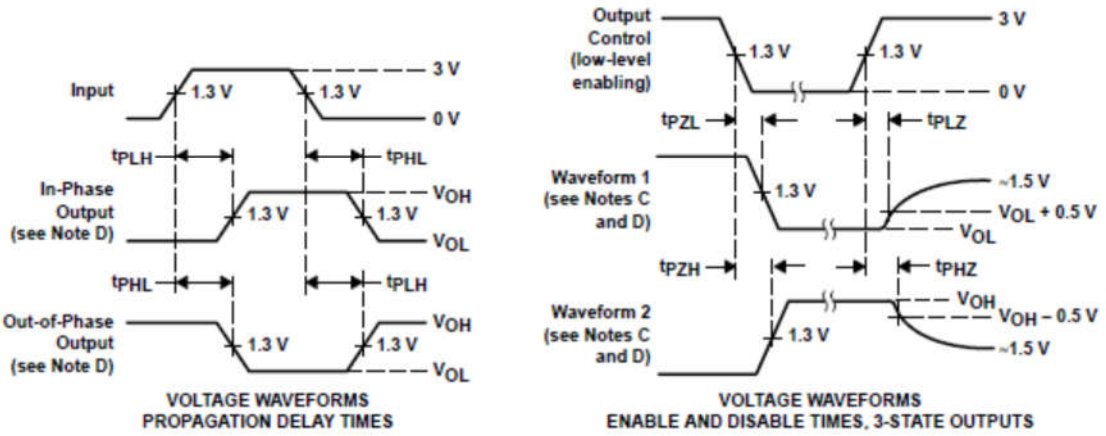
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$; t_r and $t_f \leq 7$ ns for Series 54/74 devices and t_r and $t_f \leq 2.5$ ns for Series 54S/74S devices.
F. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES







NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ~ 50 Ω, t_r ≤ 1.5 ns, t_f ≤ 2.6 ns.
G. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

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Documentation technique du TL081 (extrait)

TL081

General purpose JFET single operational amplifiers

Features

- Wide common-mode (up to V_{CC}^+) and differential voltage range
- Low input bias and offset current
- Output short-circuit protection
- High input impedance JFET input stage
- Internal frequency compensation
- Latch-up free operation
- High slew rate: 16 V/µs (typ)

Description

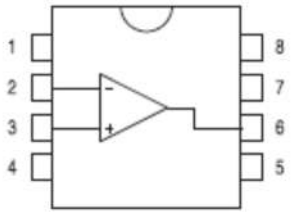
The TL081, TL081A and TL081B are high-speed JFET input single operational amplifiers incorporating well matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

N
DIP8
(Plastic package)

D
SO-8
(Plastic micropackage)

Pin connections
(top view)



1 - Offset null 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Offset null 2
6 - Output
7 - V_{CC}^+
8 - N.C.

1 Schematic diagram

Figure 1. Schematic diagram

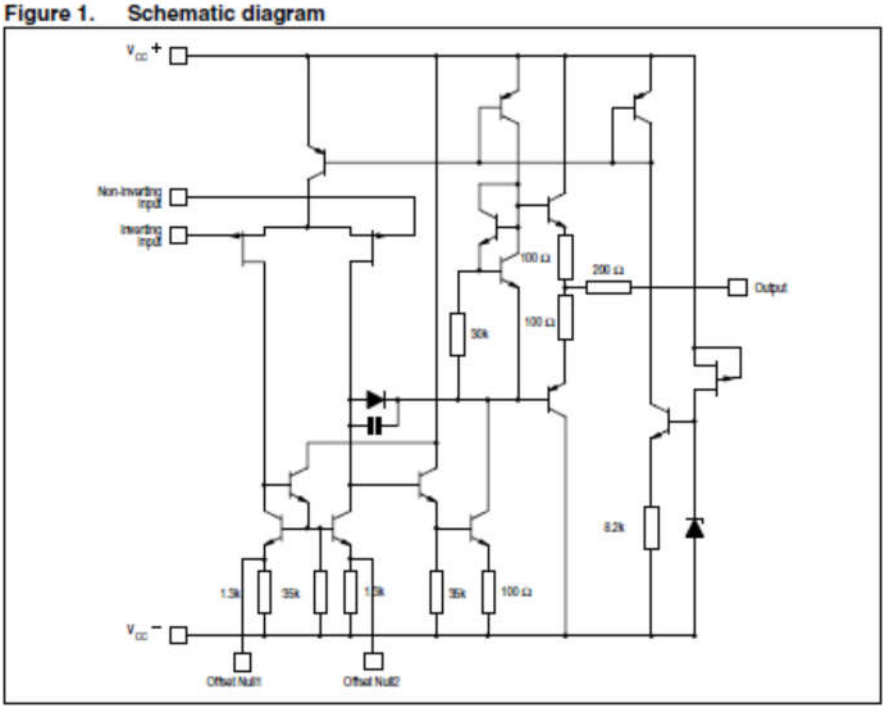
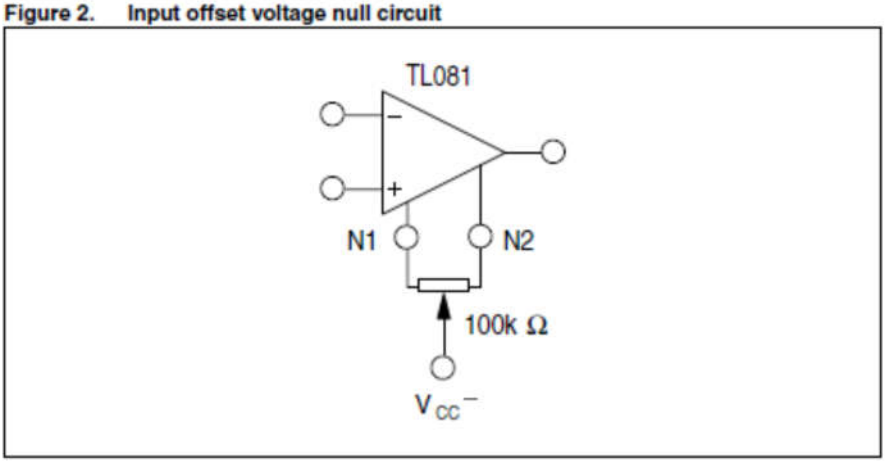


Figure 2. Input offset voltage null circuit



2 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	TL081I, AI, BI	TL081C, AC, BC	Unit
V_{CC}	Supply voltage (1)	±18		V
V_{in}	Input voltage (2)	±15		V
V_{id}	Differential input voltage (3)	±30		V
P_{tot}	Power dissipation	680		mW
	Output short-circuit duration (4)	Infinite		
T_{stg}	Storage temperature range	-65 to +150		°C
R_{thja}	Thermal resistance junction to ambient(5) (6) SO-8 DIP8	 125 85		°C/W
R_{thjc}	Thermal resistance junction to case(5) (6) SO-8 DIP8	 40 41		°C/W
ESD	HBM: human body model(7)	500		V
	MM: machine model(8)	200		V
	CDM: charged device model(9)	1.5		kV

1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
3. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. Short-circuits can cause excessive heating and destructive dissipation.
6. Rth are typical values.
7. Human body model: 100 pF discharged through a 1.5kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
8. Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
9. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

Table 2. Operating conditions

Symbol	Parameter	TL081I, AI, BI	TL081C, AC, BC	Unit
V_{CC}	Supply voltage range	6 to 36		V
T_{oper}	Operating free-air temperature range	-40 to +105	0 to +70	°C

3 Electrical characteristics

Table 3. V_{CC} = ±15V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	TL081I, AC, AI, BC, BI			TL081C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input offset voltage (R_s = 50Ω) T_{amb} = +25°C TL081 TL081A TL081B $T_{min} \le T_{amb} \le T_{max}$ TL081 TL081A TL081B		 3 3 1	 10 6 3 13 7 5		 3	 10 13	mV
DV_{io}	Input offset voltage drift		10			10		µV/°C
I_{io}	Input offset current (1) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		5	100 4		5	100 10	pA nA
I_{ib}	Input bias current (1) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		20	200 20		20	400 20	nA
A_{vd}	Large signal voltage gain (R_L = 2kΩ, V_o = ±10V) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	50 25	200		25 15	200		V/mV
SVR	Supply voltage rejection ratio (R_S = 50Ω) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	80 80	86		70 70	86		dB
I_{CC}	Supply current, no load T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		1.4	2.5 2.5		1.4	2.5 2.5	mA
V_{icm}	Input common mode voltage range	±11	+15 -12		±11	+15 -12		V
CMR	Common mode rejection ratio (R_S = 50Ω) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	80 80	86		70 70	86		dB
I_{os}	Output short-circuit current T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	10 10	40	60 60	10 10	40	60 60	mA
$\pm V_{opp}$	Output voltage swing T_{amb} = +25°C R_L = 2kΩ R_L = 10kΩ $T_{min} \le T_{amb} \le T_{max}$ R_L = 2kΩ R_L = 10kΩ	10 12 10 12	12 13.5		10 12 10 12	12 13.5		V
SR	Slew rate (T_{amb} = +25°C) V_{in} = 10V, R_L = 2kΩ, C_L = 100pF, unity gain	8	16		8	16		V/µs

Table 3. V_{CC} = ±15V, T_{amb} = +25°C (unless otherwise specified) (continued)

Symbol	Parameter	TL081I, AC, AI, BC, BI			TL081C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_r	Rise time (T_{amb} = +25°C) V_{in} = 20mV, R_L = 2kΩ C_L = 100pF, unity gain		0.1			0.1		µs
K_{ov}	Overshoot (T_{amb} = +25°C) V_{in} = 20mV, R_L = 2kΩ C_L = 100pF, unity gain		10			10		%
GBP	Gain bandwidth product (T_{amb} = +25°C) V_{in} = 10mV, R_L = 2kΩ C_L = 100pF, F= 100kHz	2.5	4		2.5	4		MHz
R_i	Input resistance		10^{12}			10^{12}		Ω
THD	Total harmonic distortion (T_{amb} = +25°C), F= 1kHz, R_L = 2kΩC_L = 100pF, A_v = 20dB, V_o = $2V_{pp}$		0.01			0.01		%
e_n	Equivalent input noise voltage R_S = 100Ω, F= 1kHz		15			15		$\frac{nV}{\sqrt{Hz}}$
∅m	Phase margin		45			45		degrees

1. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

Figure 3. Maximum peak-to-peak output voltage versus frequency

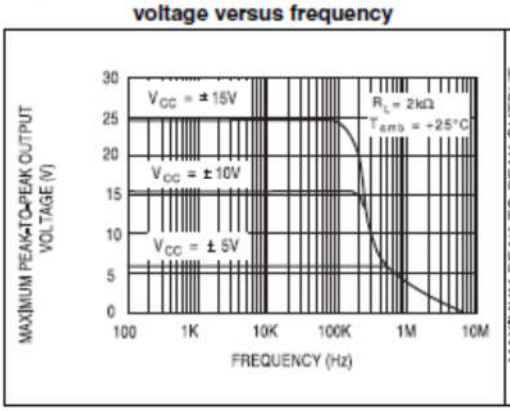


Figure 4. Maximum peak-to-peak output voltage versus frequency

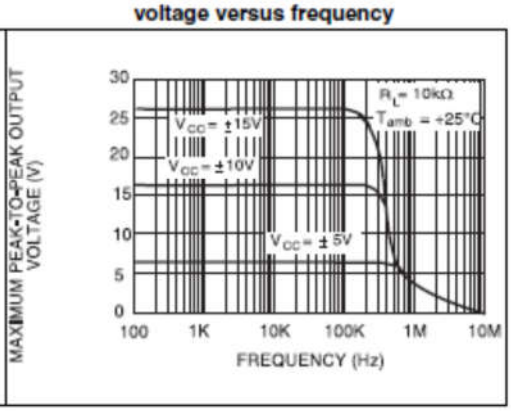


Figure 5. Maximum peak-to-peak output voltage versus frequency

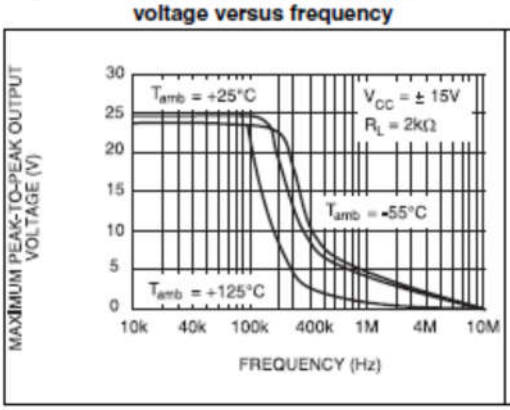


Figure 6. Maximum peak-to-peak output voltage versus free air temperature

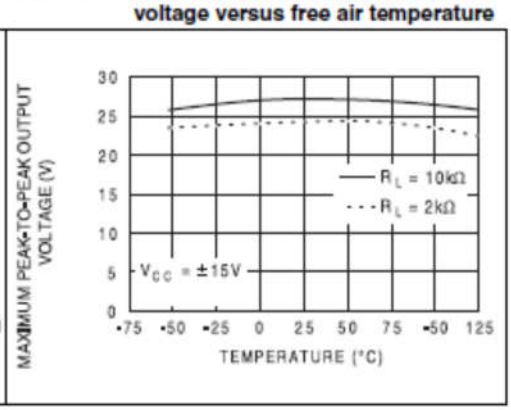


Figure 7. Maximum peak-to-peak output voltage versus load resistance

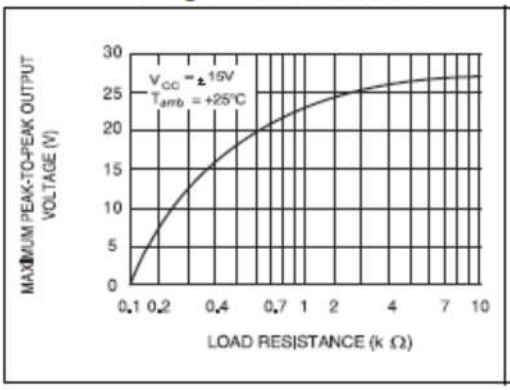


Figure 8. Maximum peak-to-peak output voltage versus supply voltage

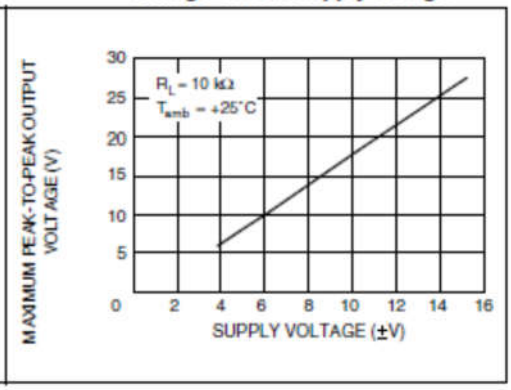


Figure 9. Input bias current versus free air temperature

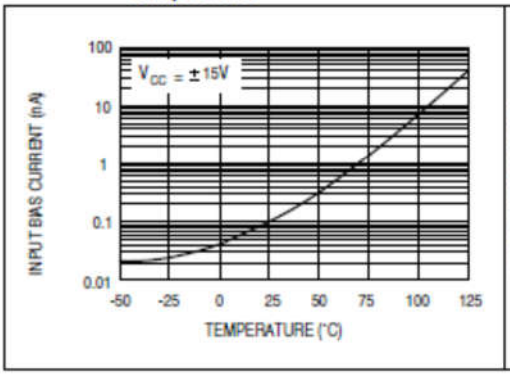


Figure 10. Large signal differential voltage amplification versus free air temp

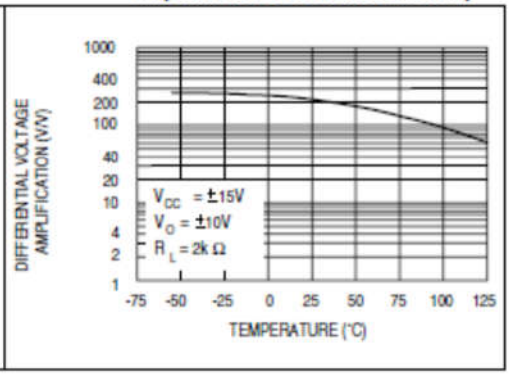


Figure 11. Large signal differential voltage amplification and phase shift versus frequency

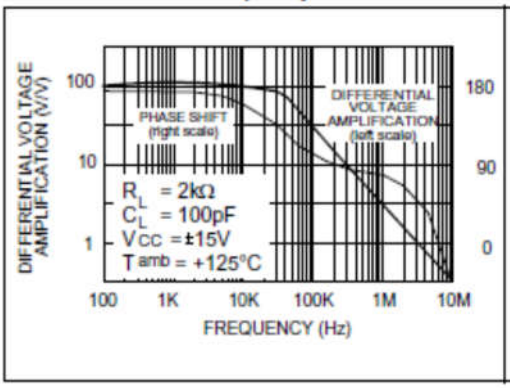


Figure 12. Total power dissipation versus free air temperature

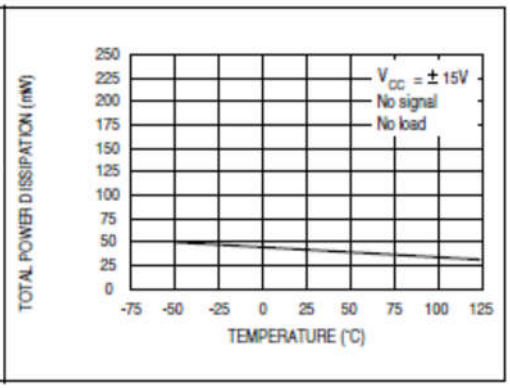


Figure 13. Supply current per amplifier versus free air temperature

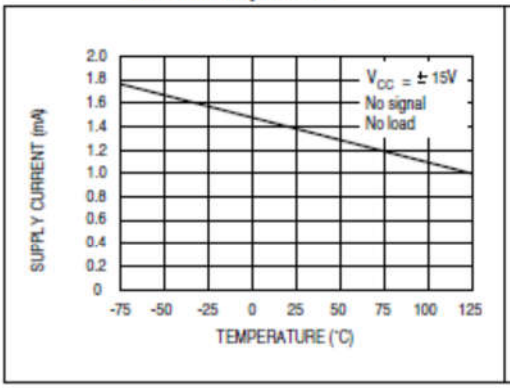


Figure 14. Supply current per amplifier versus supply voltage

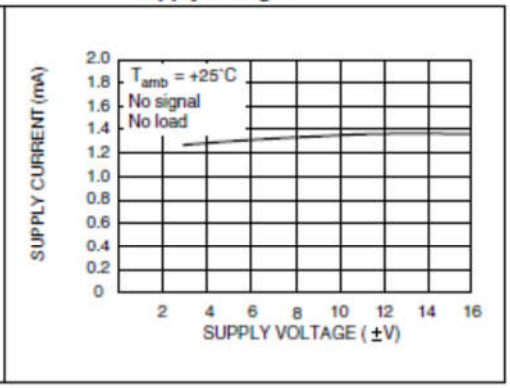


Figure 15. Common mode rejection ratio versus free air temperature

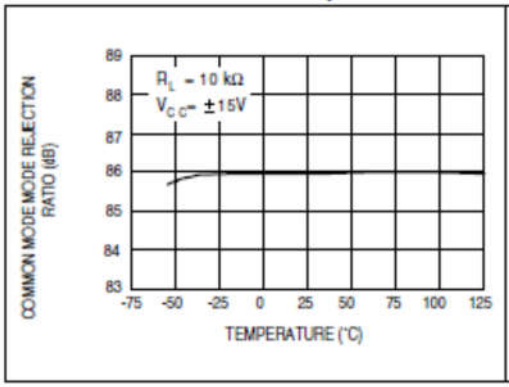


Figure 16. Equivalent input noise voltage versus frequency

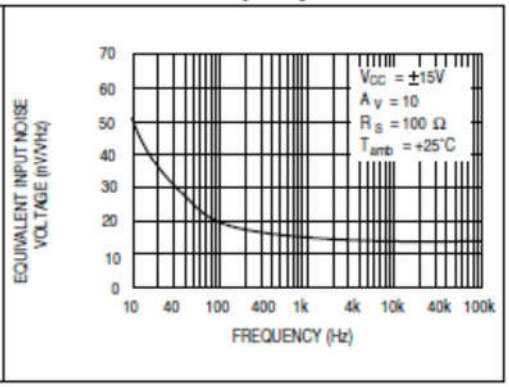


Figure 17. Output voltage versus elapsed time

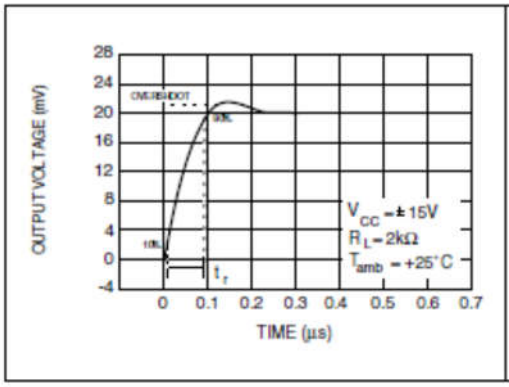


Figure 18. Total harmonic distortion versus frequency

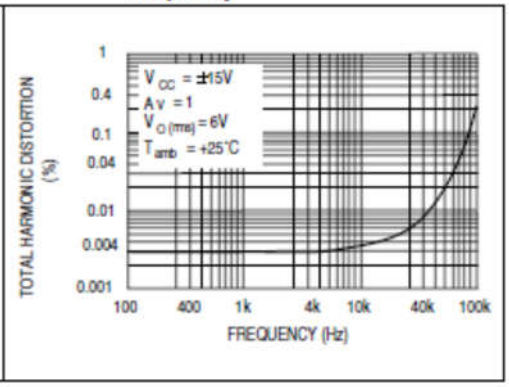


Figure 19. Voltage follower large signal pulse response